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| 10/001,719 | 11/02/2001 | Nigel C. Paver | INTL-0650-US (P12391) | 3525 |

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Timothy N. Trop
TROP, PRUNER & HU, P.C.
STE 100
8554 KATY FWY
HOUSTON, TX 77024-1805

| EXAMINER | |
|---|---|
| GERSTL, SHANE F | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/001,719 | PAVER, NIGEL C. | |
| | Examiner | Art Unit | |
| | Shane F Gerstl | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-33 have been examined.

### *Papers Received*

2. Receipt is acknowledged of amendment papers submitted, where the papers have been placed of record in the file.

3. The amendment has successfully overcome the objections to the drawings as well as the 35 USC 101 and 35 USC 112 rejections to the claims, all of which have been withdrawn.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Buchholz (4,740,893).

6. In regard to claim 1, Buchholz discloses a method comprising:

   a. determining whether a register of a processor has been updated;

   b. and if the register is updated, setting an indicator bit.

[Figure 1 shows a data processing system (processor) and figure 3 shows a set of vector registers in the vector processing unit of figure 1 (see column 2, Brief Description of Drawings). Column 6, lines 7-36 show that there are indicator bits or vector change

bits (VCH) that indicate when a vector register pair has been loaded or modified (updated).]

7. In regard to claim 2, Buchholz discloses the method of claim 1 including determining whether the register has been updated by checking the indicator bit. [Figure 5b shows in step 260 that the VCH indicator bits are checked and thus it is determined whether the corresponding register pair has been updated.]

8. In regard to claim 3, Buchholz discloses the method of claim 2 wherein if the register has not been updated, refraining from transferring the contents of the register back to a memory. [Figure 5b and the abstract show that if the contents of a register (VR or vector register) have not been changed (VCH = 0) the register is not saved to memory.]

9. In regard to claim 4, Buchholz discloses the method of claim 2 including determining whether the register has been updated and if so, saving the contents of the register to memory. [See figure 5b and abstract.]

10. In regard to claim 5, Buchholz discloses the method of claim 4 including saving the register contents to memory on a context change. [The abstract and column 8, lines 16-54 show that the registers are saved on a program or context switch.]

11. In regard to claim 6, Buchholz discloses the method of claim 1 including assigning a single indicator bit as the indicator bit for a plurality of registers. [As shown above, the change bits (VCH) or indicator bits are each associated with a register pair.]

12. In regard to claim 7, Buchholz discloses an article comprising a medium storing machine-readable instructions that if executed enables a processor-based system to:

a. determine whether a register of a processor-based system has been updated;

b. and if the register is updated, set an indicator bit.

[Figure 1 shows a data processing system (processor) and figure 3 shows a set of vector registers in the vector processing unit of figure 1 (see column 2, Brief Description of Drawings). Column 6, lines 7-36 show that there are indicator bits or vector change bits (VCH) that indicate when a vector register pair has been loaded or modified (updated). These sections further show that the functionality is a direct response to instructions and figure 1, element 14 along with column 2, lines 37-43 show a memory that stores the instructions.]

13. In regard to claim 8, Buchholz discloses the article of claim 7 further storing instructions that enable the processor-based system to determine whether the register has been updated by checking the indicator bit. [Figure 5b shows in step 260 that the VCH indicator bits are checked and thus it is determined whether the corresponding register pair has been updated.]

14. In regard to claim 9, Buchholz discloses the article of claim 8 further storing instructions that enable the processor-based system to refrain from transferring the contents of the register back to a memory if the register has not been updated. [Figure 5b and the abstract show that if the contents of a register (VR or vector register) have not been changed (VCH = 0) the register is not saved to memory.]

15. In regard to claim 10, Buchholz discloses the article of claim 8 further storing instructions that enable the processor-based system to determine whether the register

has been updated and if so, save the contents of the register to memory. [See figure 5b and abstract.]

16. In regard to claim 11, Buchholz discloses the method of claim 10further storing instructions that enable the processor-based system to save the register contents to memory on a context change. [The abstract and column 8, lines 16-54 show that the registers are saved on a program or context switch.]

17. In regard to claim 12, Buchholz discloses the article of claim 10 further storing instructions that enable the processor-based system to save the contents of a plurality of registers to memory if the indicator bit is set. [As shown above, the change bits (VCH) or indicator bits are each associated with a register pair and thus on a save each set indicator or VCH bit allows for two registers' contents to be saved.]

18. In regard to claim 13, Buchholz discloses a processor comprising:

a. a register;

b. and a storage storing instructions to determine whether the register has been updated and if the register is updated, set an indicator bit.

[Figure 1 shows a data processing system (processor) and figure 3 shows a set of vector registers in the vector processing unit of figure 1 (see column 2, Brief Description of Drawings). Column 6, lines 7-36 show that there are indicator bits or vector change bits (VCH) that indicate when a vector register pair has been loaded or modified (updated). These sections further show that the functionality is a direct response to instructions and figure 1, element 14 along with column 2, lines 37-43 show a memory that stores the instructions.]

19. In regard to claim 14, Buchholz discloses the processor of claim 13 wherein said storage stores instructions that enable the processor to determine whether the register has been updated by checking the indicator bit. [Figure 5b shows in step 260 that the VCH indicator bits are checked and thus it is determined whether the corresponding register pair has been updated.]

20. In regard to claim 15, Buchholz discloses the processor of claim 14 wherein said storage stores instructions that enable the processor to refrain from transferring the contents of the register back to a memory. [Figure 5b and the abstract show that if the contents of a register (VR or vector register) have not been changed (VCH = 0) the register is not saved to memory.]

21. In regard to claim 16, Buchholz discloses the processor of claim 14 wherein said storage stores instructions that enable the processor to determine whether the register has been updated and if so, save the contents of the register to memory. [See figure 5b and abstract.]

22. In regard to claim 17, Buchholz discloses the method of claim 14 wherein said storage stores instructions that enable the processor to save the register contents to memory on a context change. [The abstract and column 8, lines 16-54 show that the registers are saved on a program or context switch.]

23. In regard to claim 18, Buchholz discloses the processor of claim 13 including a second storage to store said indicator bit. [Column 5, line 62-column 6, line 26 shows that a vector status register holds the indicator or VCH bits.]

24. In regard to claim 19, Buchholz discloses a system comprising:

a. a processor having a register;

b. and a storage to store instructions to determine whether the register has been updated and if the register has been updated, set an indicator bit.

[Figure 1 shows a data processing system (processor) and figure 3 shows a set of vector registers in the vector processing unit of figure 1 (see column 2, Brief Description of Drawings). Column 6, lines 7-36 show that there are indicator bits or vector change bits (VCH) that indicate when a vector register pair has been loaded or modified (updated). These sections further show that the functionality is a direct response to instructions and figure 1, element 14 along with column 2, lines 37-43 show a memory that stores the instructions.]

25. In regard to claim 20, Buchholz discloses the system of claim 19 including a memory and an interface between said memory and said processor. [Figure 1 shows that there is an interface from the storage (20) and the rest of the processor.]

26. In regard to claim 21, Buchholz discloses the system of claim 20 wherein said storage stores instructions that enable the processor to determine whether the register has been updated by checking the indicator bit. [Figure 5b shows in step 260 that the VCH indicator bits are checked and thus it is determined whether the corresponding register pair has been updated.]

27. In regard to claim 22, Buchholz discloses the system of claim 21 wherein said storage stores instructions that enable the processor to refrain from transferring the contents of the register back to the memory. [Figure 5b and the abstract show that if the

contents of a register (VR or vector register) have not been changed (VCH = 0) the register is not saved to memory.]

28. In regard to claim 23, Buchholz discloses the system of claim 21 wherein said storage stores instructions that enable the processor to determine whether the register has been updated and if so, save the contents of the register to the memory. [See figure 5b and abstract.]

29. In regard to claim 24, Buchholz discloses the method of claim 23 wherein said storage stores instructions that enable the processor to save the register contents to memory on a context change. [The abstract and column 8, lines 16-54 show that the registers are saved on a program or context switch.]

30. In regard to claim 25, Buchholz discloses the system of claim 19 including a second storage to store said indicator bit. [Column 5, line 62-column 6, line 26 shows that a vector status register holds the indicator or VCH bits.]

31. In regard to claim 26, Buchholz discloses the system of claim 19 including a control register to store said indicator bit and wherein said storage storing instructions and said control register are part of said processor. [Figure 1 shows that the memory (20) and the Vector Processing Unit (which has been shown in the brief Description of Drawings to hold the vector registers) are in the processor.

32. In regard to claim 27, Buchholz discloses the system of claim 19 including a plurality of registers coupled to said processor and a single indicator bit as the indicator bit for all of those registers. [As shown above there are register pairs (a plurality of registers) associated with each change or indicator bit.]

33. In regard to claim 28, Buchholz discloses the method of claim 5, further comprising not saving the register contents to memory on the context change if the register has not been updated. [Figure 5b and the abstract show that if the contents of a register (VR or vector register) have not been changed (VCH = 0) the register is not saved to memory.]

34. In regard to claim 29, Buchholz discloses the article of claim 11, further comprising instructions that enable the processor-based system to not save the register contents to memory on the context change if the register has not been updated. [Figure 5b and the abstract show that if the contents of a register (VR or vector register) have not been changed (VCH = 0) the register is not saved to memory.]

***Claim Rejections - 35 USC § 103***

35. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

36. Claims 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buchholz.

37. In regard to claim 30,

a. Buchholz discloses the processor of claim 18,

b. Buchholz does not disclose wherein said register includes said second storage. Buchholz instead shows in columns 5-6 that the second storage is in

the E-function unit, which is separate from the vector processing unit as shown in figure 1.

c. The examiner is taking Official Notice that storing indicator bits for data in a register in that register is conventional and well known in the art.

d. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Buchholz to store the change or indicator bits with the register pair that those bits are associated with since Examiner takes Official Notice that storing indicator bits of a register within that register is conventional and well known and because the bits would then be in a centralized location with the register data and updates of the data and change bits could be done simultaneously to save time.

e. Additionally, it would have been obvious to one of ordinary skill in the art at the time of invention to place the vector change bits in the register being tested for modification since it has been held that shifting the location of parts in a manner that does not affect the operation of a system is obvious. *In re Japikse* 86 USPQ 70 (CCPA 1958).

38. In regard to claim 31, Buchholz discloses the processor of claim 30, wherein said register comprises a control register. [Since the indicator bit in the register controls the storage to memory, it may be appropriately named a control register.]

39. In regard to claim 32,

a. Buchholz discloses the system of claim 25, wherein said register includes said second storage.

b. Buchholz does not disclose wherein said register includes said second storage. Buchholz instead shows in columns 5-6 that the second storage is in the E-function unit, which is separate from the vector processing unit as shown in figure 1.

c. The examiner is taking Official Notice that storing indicator bits for data in a register in that register is conventional and well known in the art.

d. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Buchholz to store the change or indicator bits with the register pair that those bits are associated with since Examiner takes Official Notice that storing indicator bits of a register within that register is conventional and well known and because the bits would then be in a centralized location with the register data and updates of the data and change bits could be done simultaneously to save time.

e. Additionally, it would have been obvious to one of ordinary skill in the art at the time of invention to place the vector change bits in the register being tested for modification since it has been held that shifting the location of parts in a manner that does not affect the operation of a system is obvious. *In re Japikse* 86 USPQ 70 (CCPA 1958).

40. In regard to claim 33, Buchholz discloses the processor of claim 32, wherein said register comprises a control register. [Since the indicator bit in the register controls the storage to memory, it may be appropriately named a control register.]

***Response to Arguments***

41. Applicant's arguments with respect to claims 1-33 have been considered but are moot in view of the new ground(s) of rejection.

42. The Examiner has included citation of the Nikhil reference used in the previous Office Action in the attached PTO-892 form at the request of the Applicant.

***Conclusion***

43. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

44. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The references cited in the previous action remain pertinent and are cited herein by reference. The following reference is cited to further show the art with respect to saving modified registers on a context switch.

US Pat No 5,974,512 to Chiba teaches a processing system that checks indicator bits to see if registers have changed and saves only the changed registers to memory on a context switch. The only difference between the disclosure and Applicant's claims is that each indicator bit identifies changes for a single register rather than a plurality.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (571) 272-4166. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
November 3, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100